

# HM6208/HM6208H Series 4-Bit CMOS Static RAM

T-4623-10

## 65536-Word x 4-Bit High Speed CMOS Static RAM

The Hitachi HM6208 and HM6208H are high speed 256k static RAMS organized as 64k-word x 4 bit. They realize high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous wherever high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6208 and HM6208H are packaged in the industry standard 300-mil, 24 pin, plastic DIP. The HM6208H is also available in a 300-mil, 24 pin, plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.

### Features

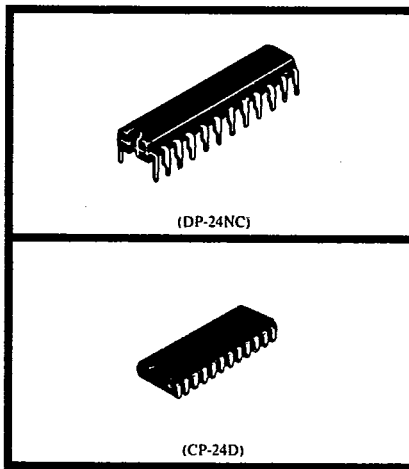
- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max.)
- Low power
  - Active: 300 mW (typ.)
  - Standby: 100  $\mu$ W (typ.)
  - 30  $\mu$ W (typ.) (L-version)
- Completely static operation requires No clock or timing strobe
- Access and cycle times are equivalent
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

### Ordering Information

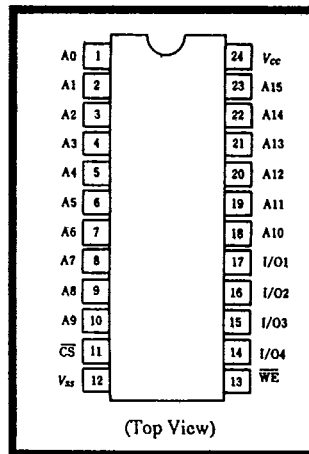
Type No.	Access Time	Package
HM6208P-35	35 ns	
HM6208P-45	45 ns	
HM6208LP-35	35 ns	300-mil
HM6208LP-45	45 ns	24-pin
HM6208HP-25	25 ns	plastic DIP
HM6208HP-35	35 ns	(DP-24NC)
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208HJP-25	25 ns	300-mil
HM6208HJP-35	35 ns	24-pin
HM6208HLJP-25	25 ns	plastic SOJ
HM6208HLJP-35	35 ns	(CP-24D)

### Pin Description

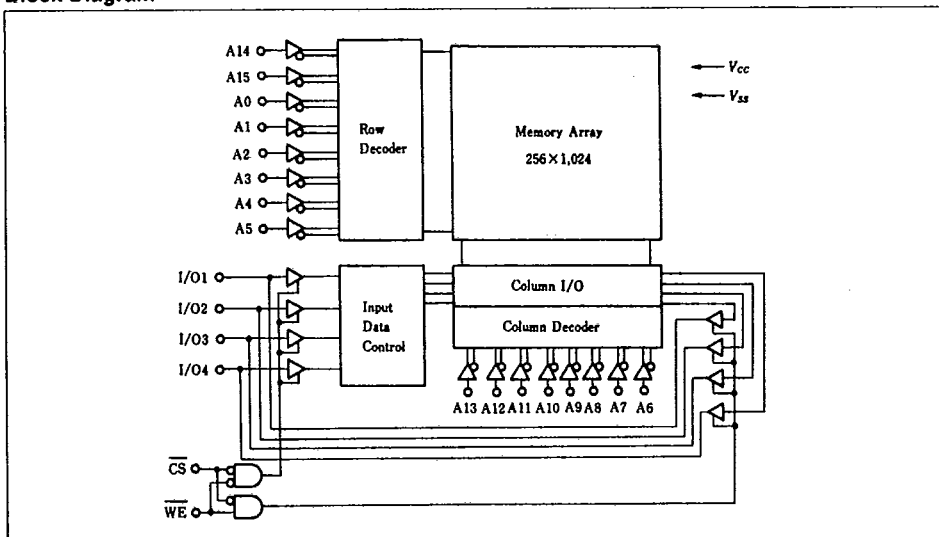
Pin Name	Function
A0 - A15	Address
I/O1 - I/O4	Input/Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground



### Pin Arrangement



**Block Diagram**



**Function Table**

CS	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	x	Not selected	I <sub>sa</sub> , I <sub>sn1</sub>	High-Z	—
L	H	Read	I <sub>cc</sub>	Dout	Read cycle
L	L	Write	I <sub>cc</sub>	Din	Write cycle

Note: x means don't care.

**Absolute Maximum Ratings**

Item	Symbol	Value	Unit
Voltage on any pin relative to V <sub>ss</sub>	V <sub>in</sub>	-0.5 <sup>*1</sup> to +7.0	V
Power dissipation	P <sub>r</sub>	1.0	W
Operating temperature range	T <sub>opr</sub>	0 to +70	°C
Storage temperature range	T <sub>stg</sub>	-55 to +125	°C
Storage temperature range under bias	T <sub>bias</sub>	-10 to +85	°C

Note: \*1. V<sub>in</sub> min = -2.5 V for pulse width ≤ 10 ns.



Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

T-46-23-10

**Recommended DC Operating Conditions** (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input high (logic 1) voltage	V <sub>HI</sub>	2.2	—	6.0	V
Input low (logic 0) voltage	V <sub>LI</sub>	-0.5 <sup>*1</sup>	—	0.8	V

Note: \*1. V<sub>LI</sub> min = -2.0 V for pulse width ≤ 10 ns.

**DC Characteristics** (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Item	Symbol	Min.	Typ. <sup>*1</sup>	Max.	Unit	Test Conditions
Input Leakage Current	I <sub>LI</sub>	—	—	2.0	μA	V <sub>CC</sub> = Max. V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output Leakage Current	I <sub>LO</sub>	—	—	10.0	μA	$\overline{CS} = V_{IH}$ V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating Power Supply Current	I <sub>CC</sub>	—	60	100	mA	$\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0 mA. Min. Cycle, Duty = 100%
Standby Power Supply Current	I <sub>SB</sub>	—	15	30	mA	$\overline{CS} = V_{IH}$ , Min. Cycle
Standby Power Supply Current "H" Version	I <sub>SB</sub>	—	20	40	mA	
Standby Power Supply Current	I <sub>SB1</sub>	—	20	2000	μA	$\overline{CS} \geq V_{CC} - 0.2$ V
Standby Power Supply Current L-Version	I <sub>SB1</sub>	—	6	100	μA	0 V ≤ V <sub>in</sub> ≤ 0.2 V or V <sub>in</sub> ≥ V <sub>CC</sub> - 0.2 V
Output Low Voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 8 mA
Output High Voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -4.0 mA

Note: \*1. Typical limits are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and specified loading.

**Capacitance** (Ta = 25°C, f = 1MHz)<sup>\*1</sup>

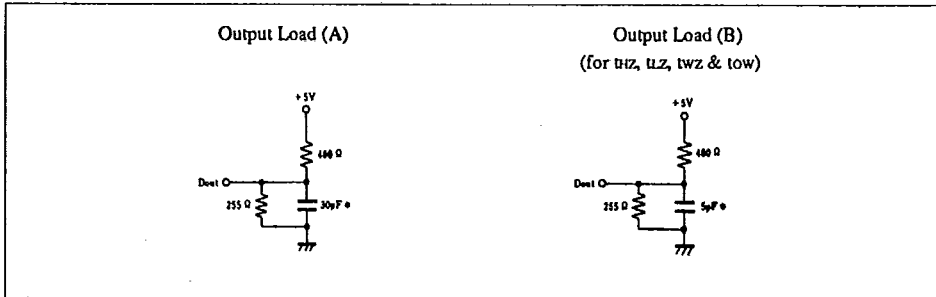
Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	6	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>io</sub>	—	10	pF	V <sub>io</sub> = 0 V

Note: \*1. This parameter is sampled and not 100% tested.

**AC Characteristics** (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted.)

**Test Conditions**

- Input pulse levels: V<sub>SS</sub> to 3.0 V
- Input and output timing reference levels : 1.5 V
- Input rise and fall times: 5 ns
- Output load: See Figures



Note: \* Including scope & jig.

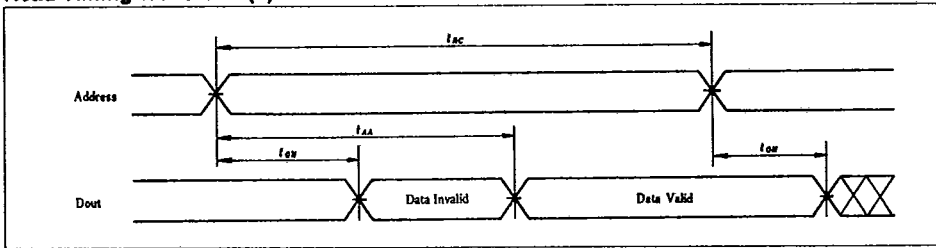


Read Cycle

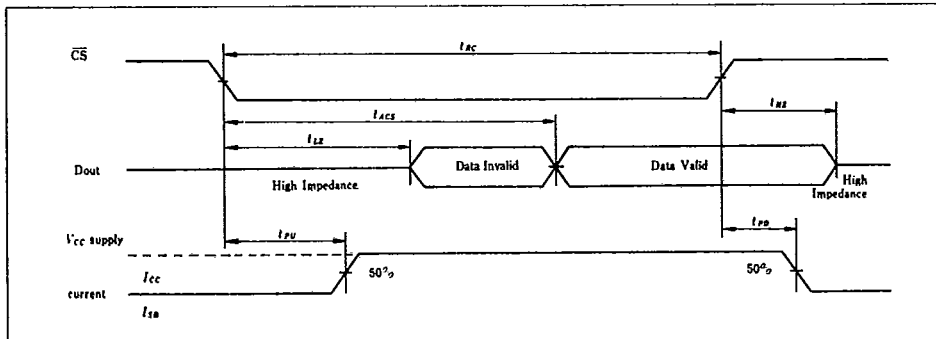
Item	Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	25	—	35	—	45	—	ns
Address Access Time	$t_{AA}$	—	25	—	35	—	45	ns
Chip Select Access Time	$t_{ACS}$	—	25	—	35	—	45	ns
Output Hold From Address Change	$t_{OH}$	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	$t_{LZ}^{*1}$	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	$t_{HZ}^{*1}$	0	12	0	20	0	20	ns
Chip Selection to Power Up Time	$t_{PU}$	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	$t_{PD}$	—	15	—	25	—	30	ns

Note: \*1 Transition is measured  $\pm 200$  mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) \*1,\*2



Read Timing Waveform (2) \*1,\*3



- Notes: \*1.  $\overline{WE}$  is high for read cycle.  
 \*2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .  
 \*3. Address valid prior to or coincident with  $\overline{CS}$  transition low.



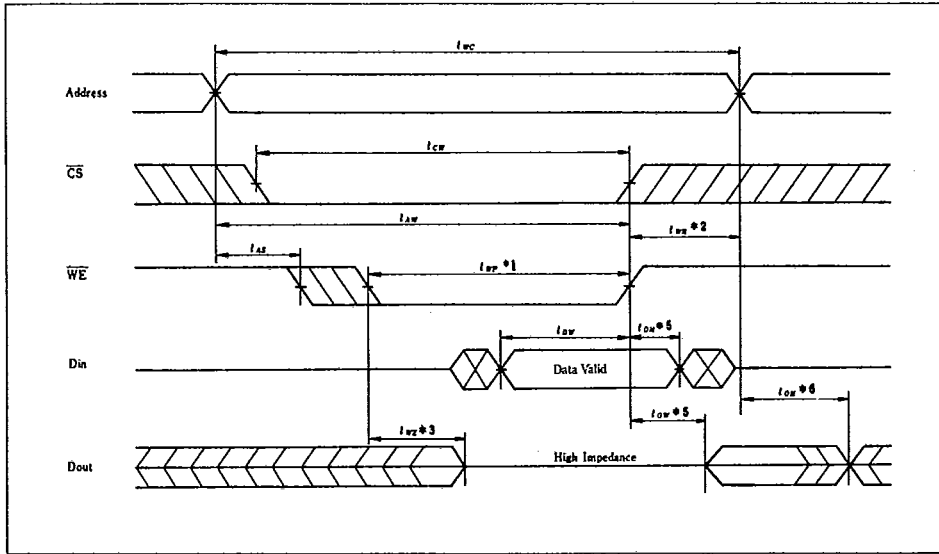
Write Cycle

T-46-23-10

Item	Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	$t_{WC}$	25	—	35	—	45	—	ns
Chip Selection to End of Write	$t_{CW}$	20	—	30	—	40	—	ns
Address Valid to End of Write	$t_{AW}$	20	—	30	—	40	—	ns
Address Setup Time	$t_{AS}$	0	—	0	—	0	—	ns
Write Pulse Width		20	—	30	—	35	—	ns
	"H" Version			$t_{WP}$				
Write Recovery Time	$t_{WR}$	3	—	3	—	3	—	ns
Data Valid to End of Write	$t_{DW}$	15	—	20	—	20	—	ns
Data Hold Time	$t_{DH}$	0	—	0	—	0	—	ns
Write Enabled to Output in High-Z	$t_{WZ}^{*1}$	0	8	0	10	0	15	ns
Output Active From End of Write	$t_{OW}^{*1}$	0	—	0	—	0	—	ns

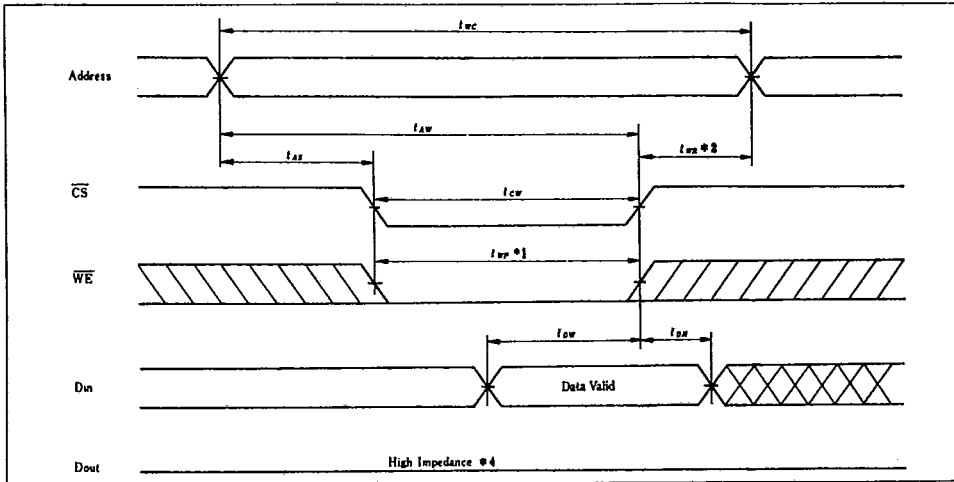
Note: \*1 Transition is measured  $\pm 200$  mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ( $\overline{WE}$  Controlled)



T-46-23-10

Write Timing Waveform (2) ( $\overline{CS}$  Controlled)



**Low V<sub>CC</sub> Data Retention Characteristics** (T<sub>a</sub> = 0 to +70°C)

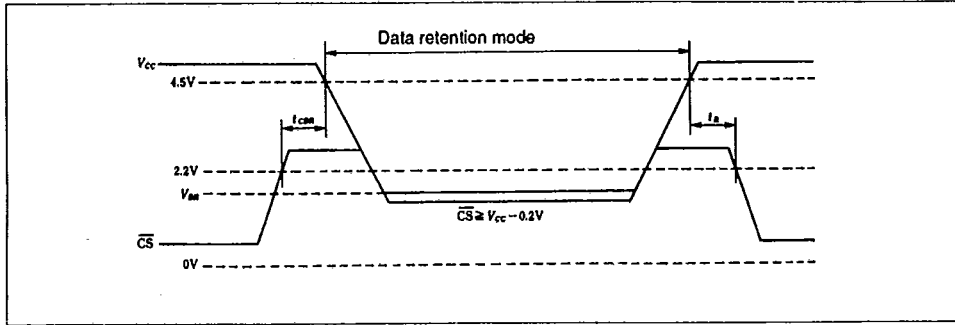
T-46-23-10

These characteristics are guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
V <sub>CC</sub> for data retention	V <sub>DR</sub>	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq V_{CC} - 0.2 \text{ V}$ or $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$
Data retention current	I <sub>CCDR</sub>	—	1	50*2	μA	
Chip deselect to data retention time	t <sub>CDR</sub>	0	—	—	ns	
Operation recovery time	t <sub>R</sub>	t <sub>RC</sub> *1	—	—	ns	

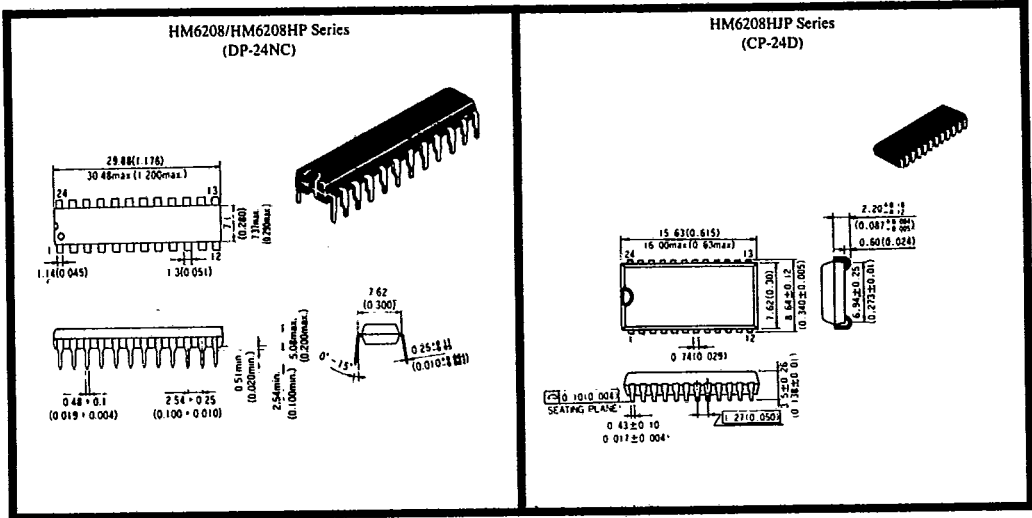
Notes: \*1. t<sub>RC</sub> = read cycle time.  
 \*2. V<sub>CC</sub> = 3.0 V.

**Low V<sub>CC</sub> Data Retention Timing Waveform**



T-46-23-10

■ PACKAGE DIMENSIONS Unit: mm (inch)



Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300